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Abstract *— Minimizing the effect of crosstalk between adjacent traces on printed circuit boards is always a challenging process, particularly in planar power devices. Many methods used to warrant sufficient electromagnetic compatibility, such as the addition of guard trace using via holes or the use of serpentine guard trace, have already been described in the literature. However, those methods may induce some issues related to the manufacturing of the PCB. In this paper, an original form of guard trace, which is composed of microstrip steps in the width, was designed and evaluated. This new guard trace acts as a microstrip filter. The electrical modeling and the simulation results of the proposed solution point out the significant reduction of the crosstalk effect (higher than 80%), while, at the same time, warranting an easier manufacturing process of the PCB.*

Keywords — Crosstalk, Radiated EMI, PCB, Planar Power Devices, Microstrip Filter.

1 INTRODUCTION

Recent advances in power electronics' applications have highlighted the continuous trend in increasing the performances in terms of energy efficiency and power densities thanks to many new innovations in semiconductor-related devices [1-3]. However, such a trend can lead to greatly affect the electromagnetic compatibility (EMC) of the power systems, partly due to higher switching frequencies of the semiconductor devices [4-6]. The compactness of the power systems is also a key criterion in today's applications. Therefore, the optimization of the layout of the printed circuit board (PCB) is of utmost importance, in particular to minimize electromagnetic interference such as the crosstalk effect on PCBs [7-8].

The crosstalk effect is due to a mutual coupling between adjacent parallel transmission lines. It can be the result of either a common impedance coupling due to the fact that several signals share a common return, or an electromagnetic field coupling which is often divided into inductive and capacitive couplings. There are 2 kinds of crosstalk: near-end crosstalk (NEXT) and far-end crosstalk (FEXT) [9].

When designing a PCB, it is of utmost importance to optimize the routing to keep the crosstalk effect at an acceptable level. Many methods, which must be in compliance with EMC standards, have been reported in the literature. One popular method consists in adding center traces in microstrips on epoxy-glass (FR4) dielectric material. A second solution consists in increasing the space between the coupled lines to reduce the parasitic electromagnetic couplings. Even if this method has recorded proven results in terms of crosstalk reduction, it leads to the increase of the size of the PCB. Two guard traces' methods have also widely been reported by many authors: via holes guard traces (VGT) and serpentine guard traces (SGT) [10-13]. It is important to remind that a guard trace is a trace routed between an "aggressor line" and a "victim line". The VGT approach is composed of conductor

lines grounded by a few plated via holes. The main issue consists in optimizing the number of via holes, and the distance between the holes, to limit the crosstalk effect [14-15]. A typical application of the SGT method consists in using horizontal and vertical guard trace sections. The horizontal section is near both the "victim" and "aggressor". The vertical section is perpendicular to the "victim". Thus, it decreases electromagnetic coupling. Although the SGT method suppresses FEXT, it also neglects most often interference caused by NEXT.

In this article, a new form of guard trace is analyzed. This new guard trace is composed of microstrip steps in the width which act as a microstrip filter. The ultimate challenge is to prove the positive impact of this microstrip filter on the crosstalk effect in planar power devices, such as in power converters' design. Section 2 of the article introduces the methodology. In particular, the limitations of the VGT and SGT methods are pointed out to show the interest of the new guard trace proposed here. Then, the electrical modeling and the simulation results are described. Section 3 of the paper discusses the main results to prove the relevance of such an approach.

2 METHODOLOGY

2.1 Presentation and Modeling of 3 Cases

As can be seen in **Figure 1**, the PCB (FR4 material; the relative permittivity and the thickness of the substrate equal 4.4 and 1.5 mm, respectively) of the power system may be composed of 2 main parts: the power part (*i.e.*, one conductor – Conductor 1 – on the PCB) and the control part (*i.e.*, another conductor – Conductor 2 – on the PCB which is in parallel with Conductor 1). The two conductors are 3 mm from each other. The aim is to insert an electromagnetic shielding track between the 2 conductors to limit the crosstalk effect. 3 cases are studied:

- A shielding layer that implements a VGT (see **Figure 1**, Case 1).

- A layer with a SGT (see **Figure 1**, Case 2).

- A shielding screen that integrates a microstrip filter also called steps' guard trace (see **Figure 1**, Case 3).

Regarding the first case (see **Figure 1**, Case 1), the PCB is composed of 3 via holes. The diameter of each hole equals 0.8 mm. In this study, the number of holes was determined from a literature review. Indeed, Chen *et al.* have recently highlighted that the optimal number of holes (N) and the interval between 2 holes depend on the length of the guard trace (L = 120 mm), the rise time of the input signal (T_R) and the transmission velocity (V_R) as expressed in equation **(1)** and equation **(2)** [14].

$$D = T_R V_R \quad (1)$$

$$N = \frac{L}{D} + 1 \quad (2)$$

From equation **(1)** and equation **(2)**, considering that the values of the T_R and V_R-parameters are equal to 300 ps and 200 m.s^{-1}, respectively, the value of the D-parameter equals 60 mm. In this article, the manufacturing process of the PCB in that case considered that the distance between 2 successive holes is equal to 59 mm.

Figure 2 shows the electrical modeling of such an electromagnetic shielding layer that implements VGT. Such a model, which is based on the linear parameters of coupled transmission lines, represents an equivalent electrical model between one conductor and the guard trace. It is important to note that the inductance and capacitance values are the same along the entire length of the conductor.

The second method (see **Figure 1**, Case 2) against radiated EMI consists in adding a serpentine guard trace between the microstrip coupled lines. This serpentine guard trace is composed of vertical and horizontal sections, and right angle bends of microstrip. Its length equals 124 mm (slightly higher than the value given in the first case because of the serpentine form). The distance between the first

conductor and the guard and the second conductor / guard distance are equal to 0.5 mm and 2 mm, respectively. As a consequence, the width of the serpentine guard trace equals 0.5 mm. This requires particular attention, especially during the manufacturing process of the PCB. In this paper, an equivalent electrical model is proposed. In particular, from a literature review, it is possible to model the right-angle bends of microstrip in the serpentine trace using inductances and capacitances. Equation **(3)** and Equation **(4)** give the formula used to extract the capacitance and inductance values [16]. In those equations, the ε_r, h and W-parameters represent the relative permittivity of the substrate (ε_r = 4.4), the thickness of the substrate (h = 1.5 mm), and the width of a conductor, respectively.

$$\frac{C}{W}[pF/m] = \begin{cases} \dfrac{(14\varepsilon_r + 12.5)\dfrac{W}{h} - (1.83\varepsilon_r + 2.25)}{\sqrt{\dfrac{W}{h}}} + \dfrac{0.02\varepsilon_r}{\dfrac{W}{h}}, \ for \ \dfrac{W}{h} < 1 \\ (9.5\varepsilon_r + 1.25)\dfrac{W}{h} + 5.2\varepsilon_r + 7, \ for \ \dfrac{W}{h} \geq 1 \end{cases} \quad (3)$$

$$\frac{L}{h}[pH/m] = 100\left(4\sqrt{\frac{W}{h}} - 4.21\right) \quad (4)$$

The serpentine guard trace is composed of several vertical lines and microstrips with right angle bends. **Figure 3** and **Figure 4** give the electrical modeling of a vertical line in a SGT, and a microstrip with a right angle bend, respectively. It is important to note that the electrical modeling is assumed to be lossless. Therefore, it is only composed of L-C cells. The losses in the conductor (resistance), and the losses in the substrate (conductance) are neglected. Regarding the vertical line in a SGT, the model takes into consideration several sections of transmission lines coupled with a change in the spacing between the lines. Two coupled microstrip lines with a serpentine guard trace were simulated in the HFSS software tool for frequencies from 10 kHz to 1 GHz. The aim was to validate the relevance of the electrical modeling. As the vertical line is composed of a right angle

followed by a microstrip line, then another right angle, the effect of couplings on the line were neglected. **Table I** gives the accuracy of the modeling, depending on the capacitances and inductances, the features of the PCB (ε_r, h), and the width of a conductor (W).

Regarding the third case (see **Figure 1**, Case 3), an original form of guard trace is proposed. It is composed of several microstrip steps in the width. One microstrip has the following dimensions: 1 mm × 2 mm. The distance between 2 successive microstrips equals 20 mm. The length of this kind of shielding track equals 120 mm (the same value as Case 1). The electrical modeling can be deduced from the previous cases.

2.2 Simulation Set-up to Compare the 3 Guard Trace Strategies

The ultimate challenge of this manuscript is to get a better understanding of the influence of the guard trace strategy on the crosstalk effect. Each structure may be simulated thanks to a software tool dedicated to high-frequency electromagnetic fields. The ANSYS HFSS software tool is currently the industry standard. It offers various methods to solve most of microwave, RF, and high-speed digital applications. However, the simulation durations can be very important. In this paper, the HFSS software tool was chosen to characterize the behavior of each guard trace method in frequency domain. A lossless SPICE electrical modeling approach was also chosen to simulate their behavior in time domain. In particular, each case is considered to be equivalent to L-C cells. The losses in each conductor (resistances), and the losses in the substrate (conductance) are neglected. Such an approach is far easier and faster. Thus a qualitative analysis is discussed in this manuscript.

Figure 5 shows the electrical simulation set-up. Regarding the “aggressor” conductor, a voltage generator is used to simulate a pulse signal with an amplitude of 10 V. So, the each is to measure the impact of the “aggressor” on the “victim” conductor. Each guard trace method (*i.e.*, VGT [Case 1], SGT [Case 2], and microstrip filters [Case 3]) was subjected to the same simulation methodology.

The electrical simulation outputs consist in extracting the NEXT and FEXT-parameters. It is important to note that a comparison between the results from the HFSS software tool and the SPICE electrical simulation results. The aim is to point out that those 2 approaches give approximately the same qualitative results. The electrical circuit approach can be improved by taking into consideration the lossy effect due to the conductances and resistances of the model.

3 MAIN RESULTS AND DISCUSSION

The first simulation result consists in comparing the electrical modeling and the electromagnetic simulation (HFSS software tool). **Figure 6** and **Figure 7** give the evolution of the NEXT and FEXT-parameters depending on the frequency. Those examples are given for a shielding track composed of SGT. The electrical modeling enables to reproduce the trend curve (*i.e.*, resonance frequency and width of the signal) of the NEXT or FEXT-parameter as a function of the frequency. Therefore, it is possible to compare the 3 trace guard strategies using the same method. Of course, the electromagnetic modeling (from the HFSS software tool) is much more precise, but the computing time in that case is higher.

Figure 8 and **Figure 9** give the evolution of the NEXT and FEXT-parameters depending on the frequency. In both cases, each parameter represent a relative attenuation, *i.e.* a ratio between the received wave and the emitted wave. **Table II** sums up the peak values of the NEXT and FEXT parameters for the 3 trace guard methods. From **Table II**, comparing with the results without guard trace, the new form of guard trace (*i.e.*, Case 3) exhibits the best relative diminution of the FEXT-parameter (*i.e.*, about 70%) whatever the frequency range (i.e., from 10 kHz to 600 MHz, and from 610 MHz to 800 MHz). Regarding the NEXT-parameter, the VGT method is a good solution, whatever the frequency range. However, the original form of guard trace (*i.e.*, Case 3) exhibits better results (relative diminution of the NEXT-parameter about 84%) for frequencies between 10 kHz and

600 MHz, in comparison with the VGT approach (*i.e.*, Case 1). However, those results are slightly less effective than the SGT method (*i.e.*, Case 2). Based on the analysis of the evolution of the NEXT and FEXT-parameters, the simulation results demonstrate that the new form of guard trace proposed in this article provides highly promising results in terms of peak crosstalk reduction.

Figure 10 and **Figure 11** give the evolution of the NEXT and FEXT-parameters in time domain at 15 MHz. The aim is to compare the various guard trace strategies from the SPICE electrical modeling. It is important to note that the HFSS software tool could have been used. However, the methods used to conduct those kinds of simulations are difficult to set-up. That is the reason why, an electrical circuit approach was chosen.

From **Figure 10** and **Figure 11**, without any guard trace, it is possible to measure a peak voltage higher than 10 mV on the "victim" conductor. On average, the voltage on this conductor is not negligible. All the guard trace strategies are very helpful to significantly decrease the average value and the peak value that can be measured across the "victim" conductor. The new form of guard trace proposed in this study and the SGT method give the best results.

4 CONCLUSION

At the moment, 2 methods are particularly widely used to reduce the crosstalk phenomenon on PCBs: guard trace with via holes (VGT), and serpentine guard trace (SGT). In this paper, 2 simulation methods were used to highlight the relevance of each guard trace strategy: electromagnetic simulation (HFSS software tool), and electrical modeling (SPICE). The HFSS software tool is well-appropriated to perform a frequency analysis. However, it could be difficult to simulate the behavior of a structure in time domain because of the methods implemented in such a software tool. That is the reason why, an electrical modeling was chosen in this study.

The electromagnetic simulation results exhibited that the VGT method is a good solution to

minimize the crosstalk phenomenon for a high frequency range. The main issue consists in optimizing the number of via holes, and the distance between the holes, to limit EMI.

This article proposed also a new shielding screen strategy which is composed of an original form of guard trace. This guard trace is composed of microstrips in the width. The electromagnetic simulation results highlighted that the relative diminution (in comparison with the case without guard trace) of the peak values both for the NEXT and FEXT-parameters is optimized in a wide frequency range (*i.e.*, from 10 kHz up to 800 MHz). The crosstalk effect can be reduced by 84%. This achievement is very positive, in particular for power converters' applications, where the power signals can highly disturb the control signals of the power devices. Finally, the time domain analysis exhibited that the behavior of the new form of guard trace is approximately the same as the VGT method. Thus, the new strategy to control crosstalk recorded very positive results in terms of EMI limitations. Moreover, the PCB manufacturing is relatively simple to conduct in that case.

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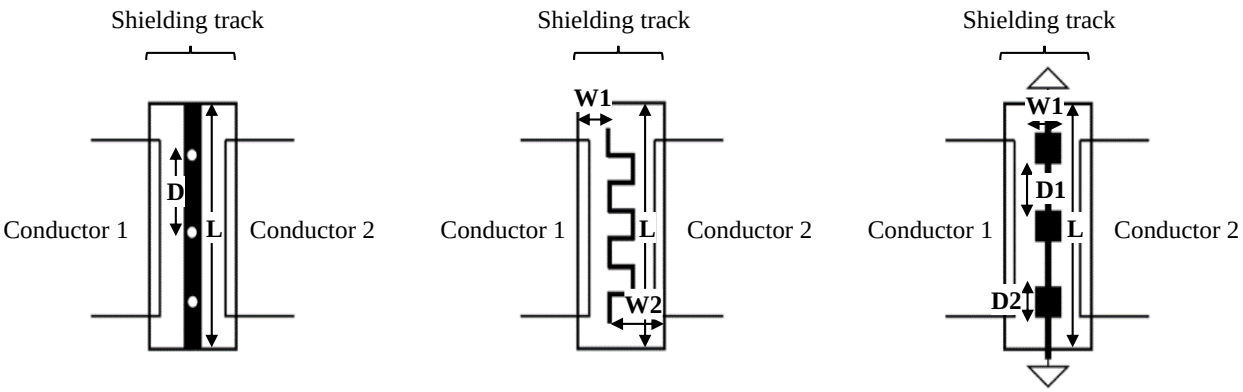
FIGURES AND TABLES



Case 1
Solution with VGT
(L = 120 mm; D = 59 mm)

Case 2
Solution with SGT
(L = 124 mm; W1 = 0.5 mm;
W2 = 2 mm)

Case 3
Solution with Microstrip filters
(L = 120 mm; D1 = 20 mm;
W1 = 1 mm; D2 = 2 mm)

Figure 1. Shielding layer between 2 conductors in parallel on a PCB: 3 cases studied

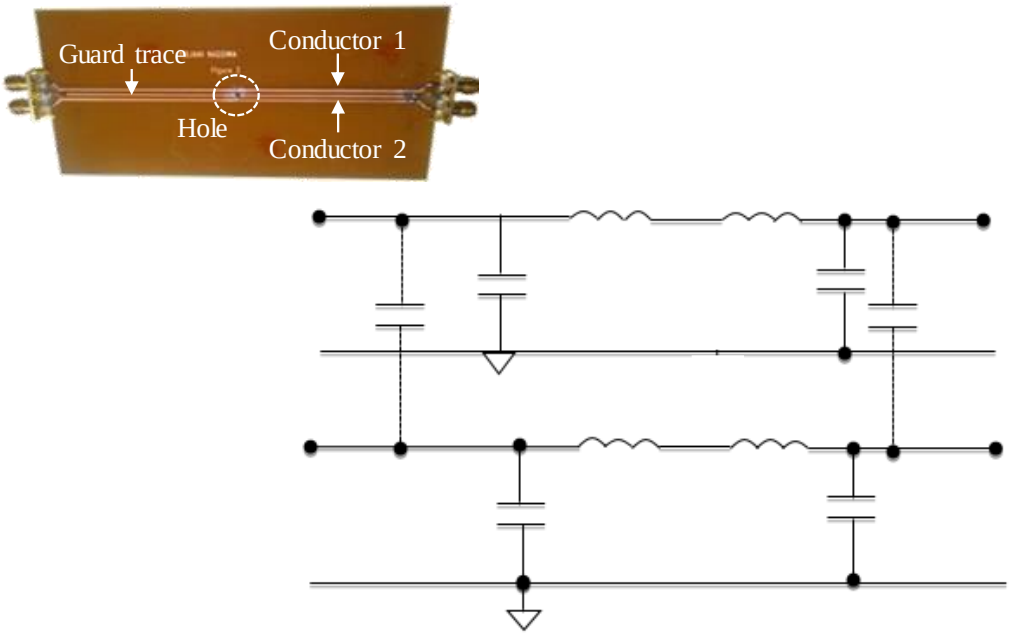


Figure 2. Equivalent electrical modeling between one conductor and the guard trace

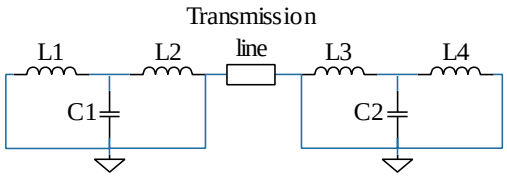


Figure 3. Electrical modeling of a vertical line in the SGT

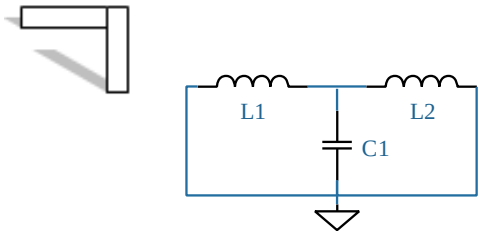


Figure 4. Electrical modeling of a microstrip with a right angle bend

TABLE I
ELECTRICAL MODEL VALIDITY LIMIT

Type of element	Accuracy	
Capacitance	5%	$1.5 \leq \varepsilon_r \leq 2.5$
		$0.1 \leq W / h \leq 5$
Inductance	3%	$0.5 \leq W / h \leq 2$

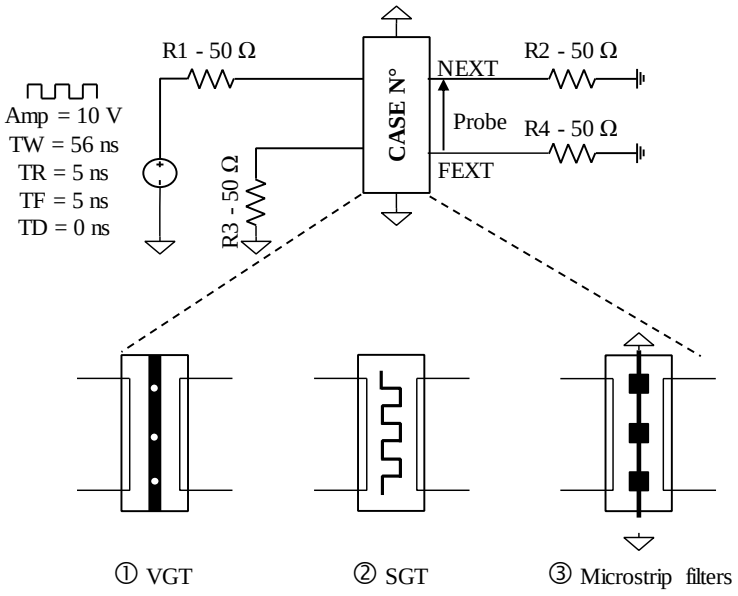


Figure 5. SPICE Electrical modeling set-up of each guard trace strategy

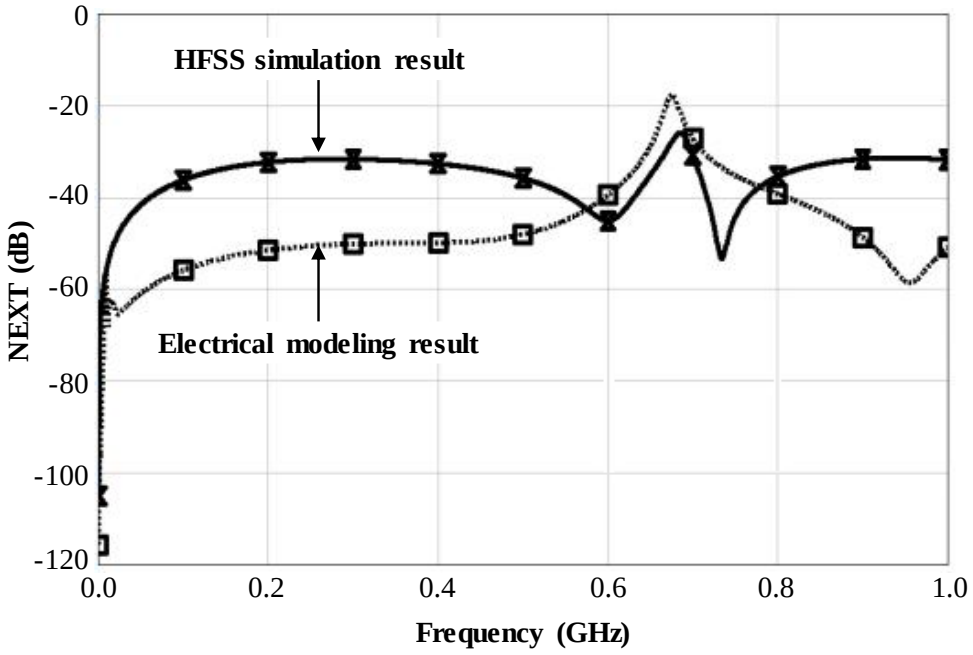


Figure 6. Evolution of the NEXT-parameter depending on the frequency for a shielding track composed of SGT. Results comparison between electromagnetic simulation and electrical circuit simulation

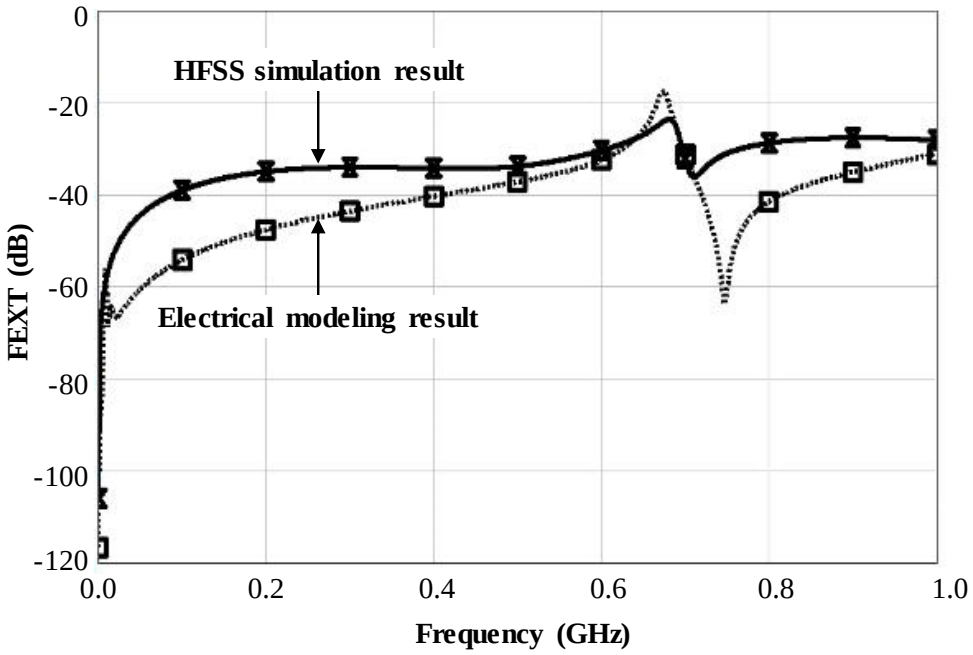


Figure 7. Evolution of the FEXT-parameter depending on the frequency for a shielding track composed of SGT. Results comparison between electromagnetic simulation and electrical circuit simulation

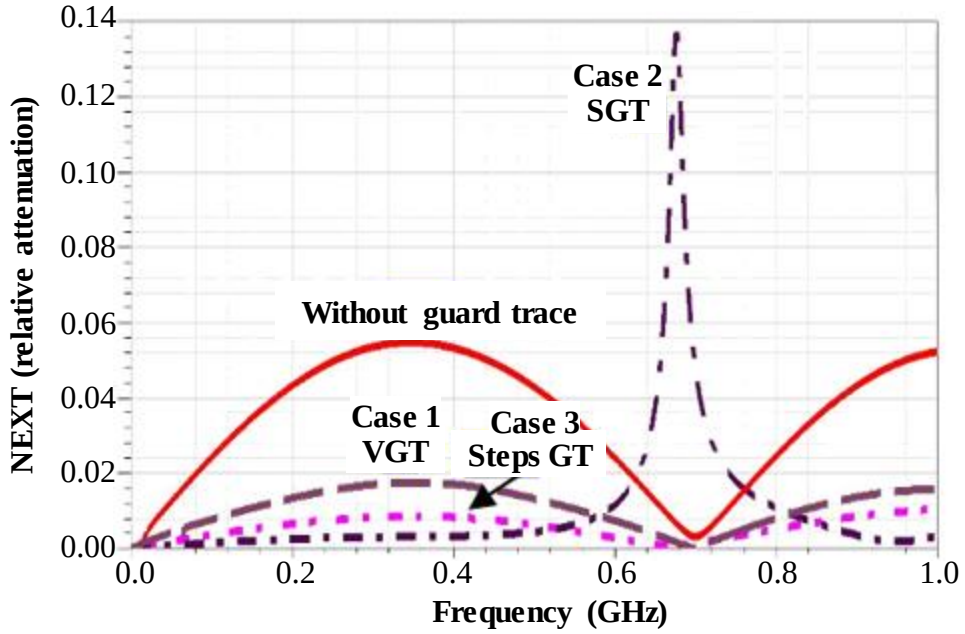


Figure 8. Evolution of the NEXT-parameter (relative attenuation) depending on the frequency. Comparison of the various guard trace strategies (HFSS design)

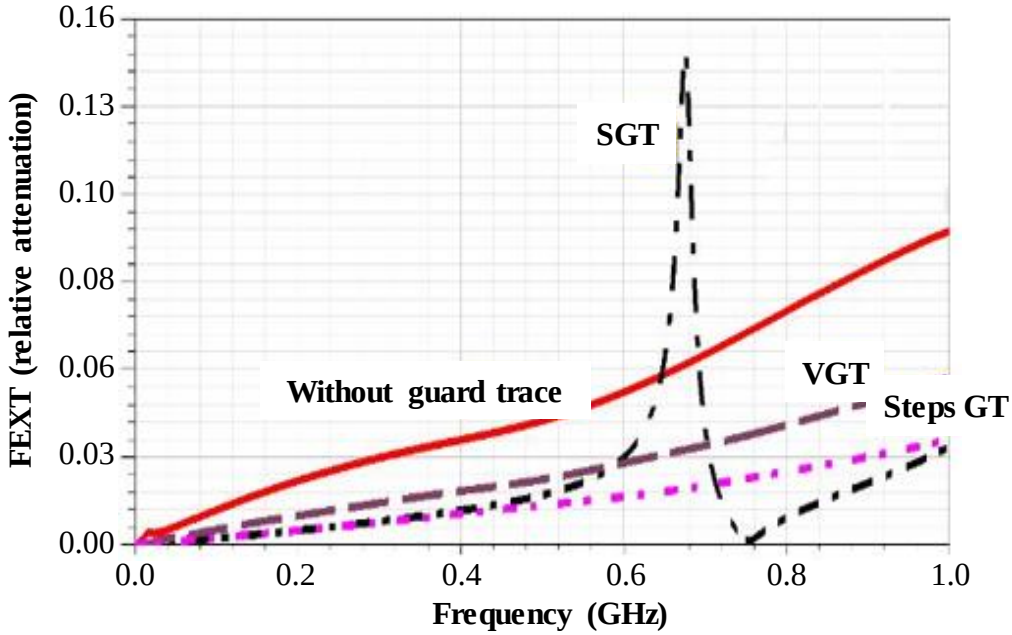


Figure 9. Evolution of the FEXT-parameter (relative attenuation) depending on the frequency. Comparison of the various guard trace strategies (HFSS design)

TABLE II
PEAK VALUES OF THE NEXT AND FEXT-PARAMETERS DEPENDING ON THE FREQUENCY RANGE

Cases	Peak-value analysis of the NEXT-parameter			
	From 10 kHz to 600 MHz	**Relative variation vs. Without guard trace**	**From 610 MHz to 800 MHz**	**Relative variation vs. Without guard trace**
Without guard trace	0.0548	-	0.005	-
Case 1 (VGT)	0.0176	-68%	0.0004	-92%
Case 2 (SGT)	0.0032	-94%	0.1359	+2,618%
Case 3 (Steps GT)	0.0086	-84%	0.0016	-68%
	Peak-value analysis of the FEXT-parameter			
Without guard trace	0.0431	-	0.0509	-
Case 1 (VGT)	0.0206	-52%	0.0265	-48%
Case 2 (SGT)	0.0204	-53%	0.1379	+171%
Case 3 (Steps GT)	0.0134	-69%	0.0155	-70%

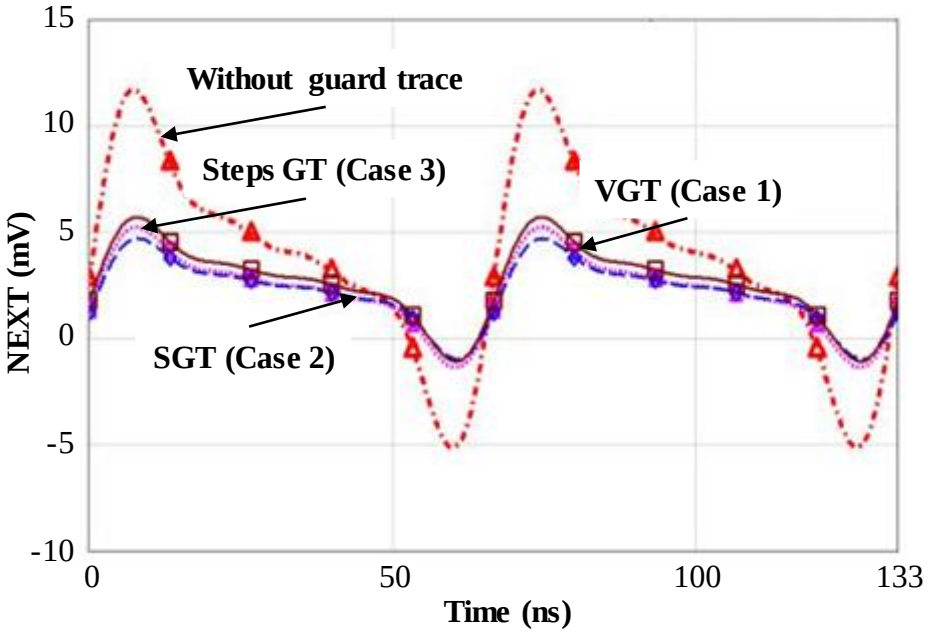


Figure 10. Evolution of the NEXT-parameter (mV) in time domain (at 15 MHz). Comparison of the various guard trace strategies (SPICE electrical modeling)

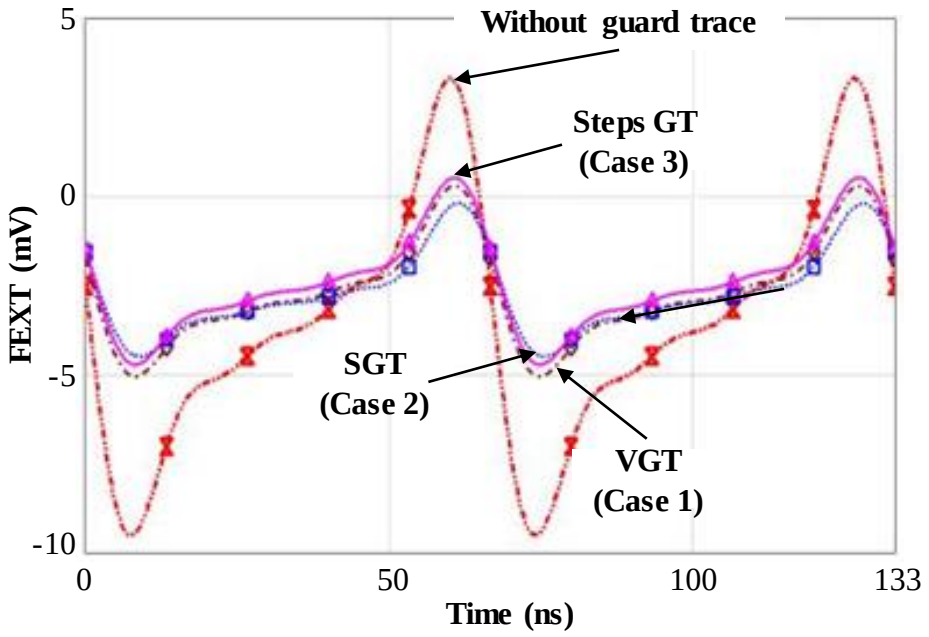


Figure 11. Evolution of the FEXT-parameter (mV) in time domain (at 15 MHz). Comparison of the various guard trace strategies (SPICE electrical modeling)

BIOGRAPHIES

Dr. Nassima Tidjani received her Magisterium degree in electromagnetic compatibility in the electrical system from the University of Laghouat in Algeria in 2007. She is currently a Ph.D. in the LTSS laboratory at the University of Laghouat. Her research interests deal with system modeling in EMC and microwaves, transmission lines, and crosstalk reduction methods.

Mr. Sébastien Bissey received the Master degree in electrical and electronic engineering from the University of Tours, Tours, France, in 2013. Since 2016, he has been with the research group on materials, microelectronics, acoustics and nanotechnology (GREMAN CNRS INSA Centre Val-de-Loire UMR 7347), where he has been hired as a Ph.D. student. His current research interests include the prediction and management of electricity in smart grids, and high efficiency power converters.

Dr. Sébastien Jacques received the Ph.D. degree in electrical engineering from the University of Tours, Tours, France, in 2010. Since 2012, he has been with the research group on materials, microelectronics, acoustics and nanotechnology (GREMAN CNRS INSA Centre Val-de-Loire UMR 7347), where he has been hired as an Assistant Professor. His current research interests include power semiconductor devices, power converters, renewable energies (photovoltaics) and reliability of power devices and systems.

Prof. Jean-Charles Le Bunetel received the Ph.D. degree in electrical engineering from the University of Le Havre, LEPII laboratory, Le Havre, France, in 1997. He is currently a full Professor at the University of Tours in France. In particular, he is a member of the research group on materials, microelectronics, acoustics and nanotechnology (GREMAN CNRS INSA Centre Val-de-Loire UMR 7347). His research interests include power electronics, power converter topologies, EMI modeling, and associated EMC problems.