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RESEARCH ARTICLE

Co-Designed Agile Feed Network for a Polarization Tunable 15 GHz Antenna All-Integrated on Silicon

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ABSTRACT This article presents an all-integrated agile feeding network at 15 GHz enabling the polarization agility of a dual-fed patch antenna, allowing the switching between LHCP (Left Hand Circular Polarized), H-LP (Horizontal Linear Polarized) and V-LP (Vertical Linear Polarized) configurations. Semiconductor Distributed Doped Areas (ScDDAs) are used with an adequate size for the global function optimization and for integrated tunability on a High Resistivity Silicon (HR Si) substrate as variable shunt resistors in the attenuators. Each component of the system has been separately analyzed in small and large signal setups to highlight the relevance of the ScDDAs in this use case. The antenna and its reconfigurable feeding network are designed as a whole in a single process flow. The device allows for an analog control and high polarization contrast interpolating between H-LP, V-LP and LHCP polarizations. The high integrability, low bias voltage, manufacturing simplicity and tuning range of this device without sacrificing the antenna frequency is matching the needs of compacity, agility and robustness of next generation communication and RADAR systems.

INDEX TERMS Antennas, attenuators, polarization, PIN diode, reconfigurable, ScDDA, tunable.

I. INTRODUCTION

Adding agile features to antennas allows for breakthroughs in compacity and efficiency of communication and RADAR systems. These innovations include frequency tunability [1], beam steering [2], and polarization tunability [3].

A polarization tunable antenna can be reconfigured to compensate for parasitic effects from its surroundings and correct misalignment losses to optimize throughput in a communication device. In a RADAR system, such tunability

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adds a new parameter to optimize sensitivity, to improve echo power and to reject jamming signals. This feature can be implemented using diverse tuning elements, such as varactor diodes [2], [3], lumped PIN diodes [4], ScDDAs (Semiconductor Distributed Doped Areas) [1], MEMS capacitors [5], MEMS switches [6], or liquid crystals [7] by placing them on the feeding line or directly on the radiating surface.

A major advantage of ScDDAs is their integration without packaging nor soldering, removing the parasitic effects associated with lumped diodes and MEMS with an optimized size of the doped areas to avoid impedance mismatch, both

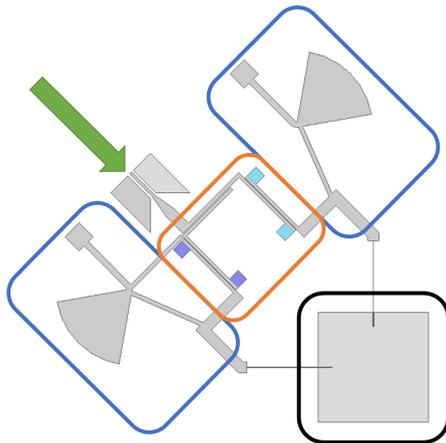


FIGURE 1. Overview of the feed network and antenna, including subsections. The N^+ doped areas for each ScDDA is highlighted in shades of blue inside the orange area.

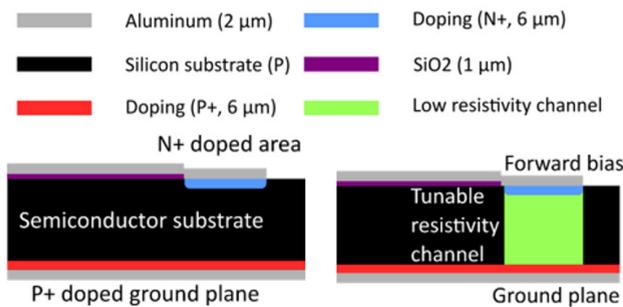


FIGURE 2. Different states of ScDDAs through (a) equilibrium to (b) forward biased configuration [8].

limiting the maximum frequency of devices using them. This technology allows the antenna to reach 15 GHz while keeping manufacturing complexity low compared to the integrated MEMS or FET approach as it only requires 2 masks (front side N^+ doping and aluminum deposition) compared to the many complex steps of MEMS or FET manufacturing.

High linearity is also an important figure of merit of ScDDAs because of the location of the active device right behind the antenna, where the RF power level is very high in a transmitter use case.

In this article, a novel three-polarization-states patch antenna all-integrated on silicon in Ku-band is proposed, taking advantages of ScDDA concept avoiding additional lumped components and allowing monolithic integration of the whole front-end. This article also presents for the first time the large signal properties of ScDDAs, validating their use in high power environments.

This study will present in detail the design considerations, simulated and measured performance of the attenuators, feeding network as well as the whole device in S parameters and emission, followed by a discussion on possible improvements and highlighting the relevance of new ScDDAs in integrated RF systems.

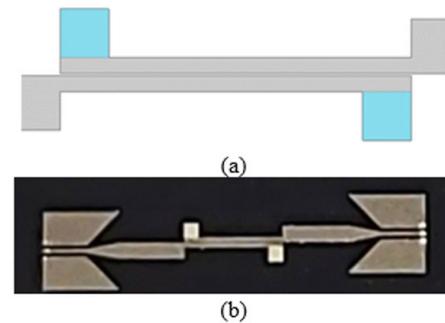


FIGURE 3. (a) Model and (b) manufactured prototype of the reflection attenuator used in the feeding network. On the model, the metallic areas are in grey, the N^+ doped areas are drawn in blue.

II. DEVICE OVERVIEW

The proposed reconfigurable antenna consists of 3 subsections, as depicted in Fig. 1:

- The input port shown as a green arrow, with a coplanar waveguide to microstrip transition to connect to the GSG probe.
- The feeding network containing 3 proximity couplers with a 90° phase shift and 3 dB of amplitude balance (in the orange-outlined area) and attenuators with ScDDAs in shades of blue.
- The dual-fed patch antenna (in the black-outlined area).
- The bias pads isolated from the RF path by quarter wave radial stubs (in the blue-outlined area).

The three states are obtained by applying a 0 V bias to the attenuators for Left-Handed Circular Polarization (LHCP) state and applying a -1 V bias, i.e. a 1 V forward bias voltage for the ScDDAs, with regards to the ground plane to each attenuator alternatively to achieve Horizontal Linear Polarized (H-LP) and Vertical Linear Polarized (V-LP) states.

A. OVERVIEW

The coupler following the input port divides the input signal in two signals of equal amplitude with a 90° phase difference. Each signal is then fed into a reflection attenuator before feeding the antenna by the corresponding orthogonal port. Each reflection attenuator consists of a $90^\circ/3\text{dB}$ coupler loaded on direct and coupled outputs by ScDDAs acting as tunable resistors. These diodes are biased by applying a voltage between the ground plane, the DC pads, and the input port. Doing so will modulate the input power of each feeding line of the antenna, allowing polarization tunability. The DC pads are isolated from the RF signal by the radial stubs in the blue squares. A similar attenuator using a branch line coupler topology has been demonstrated separately in previous works showing excellent attenuation performance and integrability [9].

Each of the components will be presented separately to demonstrate their performances before exposing the characteristics of the whole system.

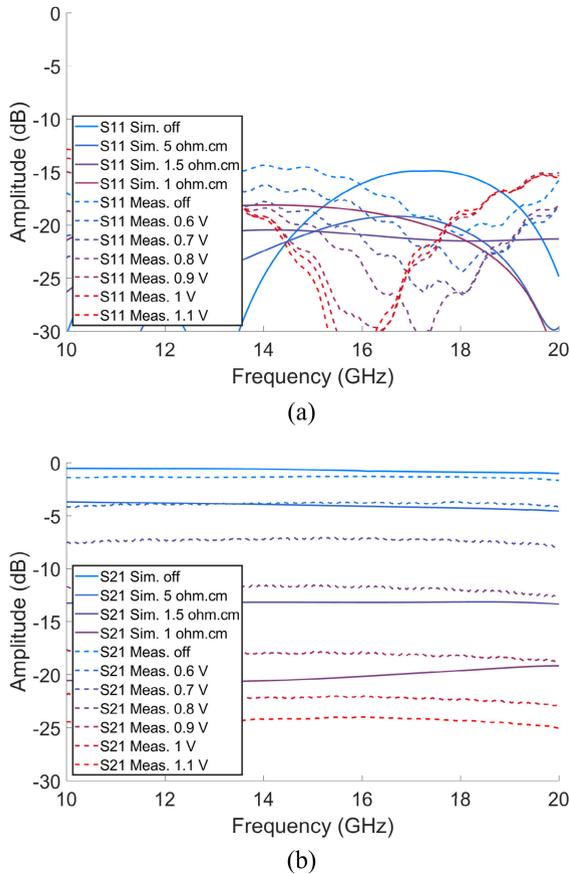


FIGURE 4. Simulated and measured performance in (a) reflection and (b) transmission of the attenuator in various biased states.

B. MANUFACTURING PROCESS AND SIMULATION FRAMEWORK

The whole device is designed on a 350 μm-thick P-type High Resistivity silicon (HR-Si) substrate with a resistivity of 2500 Ω.cm and dielectric constant of 11.9. Front side N⁺ Doping is applied by etching the oxide layer and using a Boron solgel. The doping is selectively applied by using a dedicated mask. The doping depth is 6 μm and the density is estimated to 1e20 cm⁻³ at the surface.

Back side P⁺ doping is applied on the whole wafer using ion implantation, with an estimated depth of 6 μm and a surface dopant density of 2e19 cm⁻³.

Aluminum is used for the metal layers, with a thickness of 2 μm using PVD (Physical Vapor Deposition). Only the front side of the wafer is etched using a dedicated mask. The back side of the wafer is covered in Aluminum. A summary of the structure and the typical dimensions of the diode is presented in Fig. 2.

Ansys HFSS was used for the full wave 3D simulations. To simulate the volumetric changes in the properties of the substrate during the ScDDAs commutation, a cuboid channel hypothesis is used. A separate material with a variable loss factor tan δ is defined in the volume under each doped surface. The formula describing the evolution of tan δ in a silicon

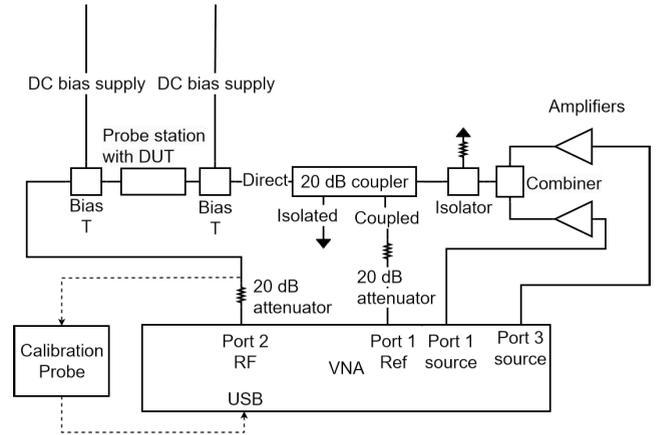


FIGURE 5. Linearity test bench overview diagram.

substrate with respect to the frequency *f*, resistivity ρ, and substrate permittivity ε₀.ε_r is shown in (1).

$$\tan \delta = 0.0018 + \frac{1}{2\pi \cdot f \cdot \rho \cdot \epsilon_0 \cdot \epsilon_r} \quad (1)$$

The performance of the device under different bias conditions is obtained by changing the resistivity of the substrate from 2500 Ω.cm (wafer resistivity) to 1 Ω.cm (value of the substrate resistivity under high bias estimated from previously manufactured devices) to model the direct bias effects on the substrate.

C. INTEGRATED DIODES AND REFLECTION ATTENUATORS

The integrated tunable resistors used as attenuator loads are implemented with N⁺PP⁺ integrated diodes using ScDDAs. The voltage applied to the pads and input port is routed to the diodes and allows for the analog control of the absorption.

The HFSS model and photograph of the attenuator are shown in Fig. 3. The coupled lines are 80 μm wide, 1.8 mm long and separated by a 12-μm gap. Doped areas are squares with 300 μm side. The simulated and measured performances of the attenuator are described in Fig. 4. The reflection coefficient is measured under 10 dB in all states from 10 GHz to 20 GHz while the attenuation range is measured from 1 dB to 25 dB from 10 GHz to 20 GHz.

The device has been tested under the linearity test bench setup built with the support of Rhodes & Schwartz. The setup includes two Superapex SAC1256 15 GHz amplifiers (gain: 20 dB, P1dB: 38 dBm), three DC power supplies to bias the amplifiers and the device under test, the R&S ZVA67 vector network analyzer and its NRP18S-25 power calibration probe, a probe station using 67A GSG 150 DP N probes from GGB Industries, as well as a power combiner, an isolator, a 20-dB coupler and two bias Tee to bring the DC bias to the DUT. An overview of the setup is presented in Fig. 5, as well as a photograph in Fig. 6.

The test bench functions as follows. The VNA signal from ports 1 and 3 is amplified through the amplifiers and recombined. An isolator protects the amplifiers from

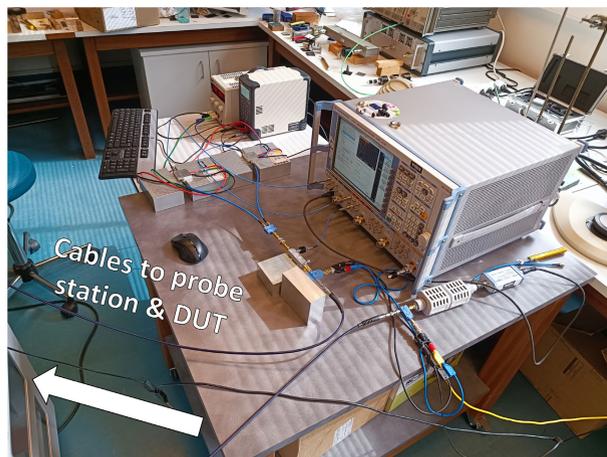


FIGURE 6. Linearity test bench photograph. The white arrow shows the direction of the probe station with DUT.

reflections from the DUT. The signal then passes through a 20 dB coupler to sample the signal out of the amplifiers in the VNA port 1 reference port and control their actual output. The remaining signal then enters the input bias Tee where the RF signal is combined to a DC bias voltage from a DC power supply to control the DUT state. The DC+RF output of the bias Tee is connected to the probe station where a GSG probe feeds the input signal to the DUT. The transmitted signal then outputs the probe station by the second probe before entering the output bias Tee that applies the DC bias to the output port. The RF signal then passes through a 20-dB attenuator to protect the VNA reception port before entering its port 2. During the power calibration phase, the VNA port is replaced by a calibration probe and the Tees are connected together. Comparing the sampled signal from the 20 dB coupler to the received signal on port 2 gives us the power dissipation through the DUT.

The maximum power possible to be calibrated using this setup is 14 dBm as the power loss between the DUT and the calibration probe cannot be compensated by calibration in this configuration. The datasheet of the cables specify 6 dB of insertion loss at 15 GHz. Consequently, all output powers presented in the figures are underestimated by 6 dB. Lower loss cables could be used in the future to improve the dynamic range.

In order to measure the third order intermodulation curve, the amplifiers output a signal with a small frequency offset. The lower tone frequency is set to 15 GHz on port 1, and the upper tone with an offset of 10 MHz on port 3.

The test bench was validated using HSMP-482 lumped diodes. The large signal curves obtained with the test bench corresponds closely with the curves provided by the manufacturer at 1.5 GHz, ensuring the accuracy of the following measurements.

The measured performance exposed in Fig. 7 (a) shows no compression under any bias condition. Fig. 7 (b) shows

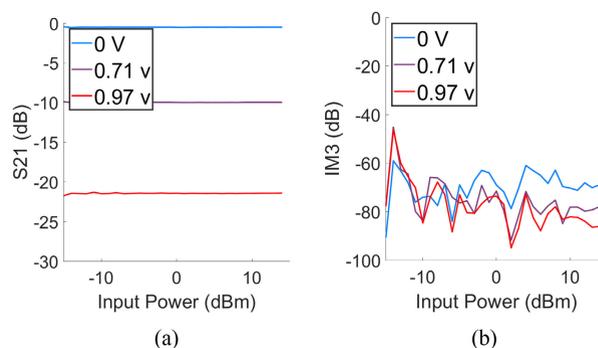


FIGURE 7. (a) Measured S_{21} at 15 GHz through the attenuator under various bias conditions with regards to input power. (b) Measured third order intermodulation product relative power through the attenuator with regards to input power in 3 different states.

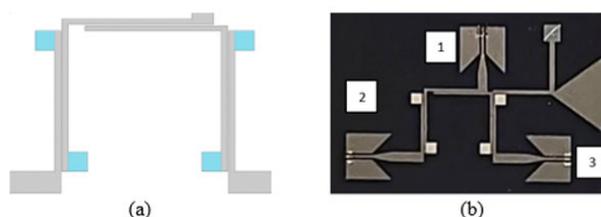


FIGURE 8. (a) Model and (b) manufactured prototype of the feed network. On the model, the metallic areas are drawn grey, the N+ doped areas are drawn blue.

no rise of the IM3 level higher than the noise level in all conditions.

Overall, the measurements validate the attenuator performance for the application as a control device in the feeding network.

D. FEEDING NETWORK

The feeding network contains 3 parts: 2 attenuators as described in the last paragraph connected to the direct and coupled ports of a proximity $90^\circ/3$ dB coupler. An HFSS model and a photograph of the manufactured sub-device are given in Fig. 8. The input coupler is used as a power divider and a phase shifter to feed the antenna ports with the 90° phase shift required for circular polarization. Each attenuator can then be used for controlling the power reaching each port of the antenna, allowing for circular, elliptic and linear polarizations.

The measured transmission parameters towards each port when each attenuator is progressively biased is exposed in Fig. 9 and Fig. 10. As expected, the transmission towards each port is drastically reduced when the associated attenuator is biased. The maximum attenuation of 22 dB and 42 dB at 15 GHz are reached towards the ports 2 and 3 respectively, while transmission of -5 dB is measured towards each port when no attenuator is biased. However, it has been measured that a parasitic attenuation of up to 3 dB towards port 2 appears when the attenuator towards port 3 is biased, while no such effect is measured on the transmission towards the

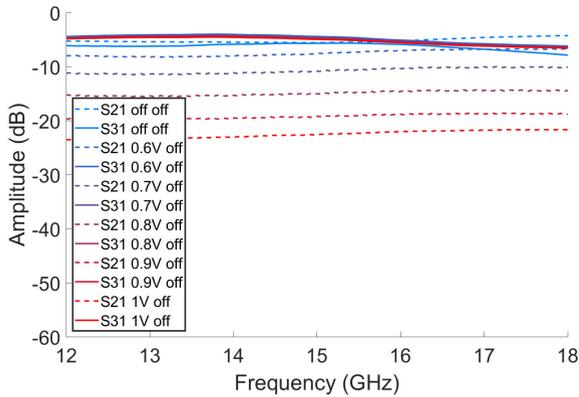


FIGURE 9. Transmission from port 1 to the ports 2 and 3 measured when the left attenuator is progressively biased.

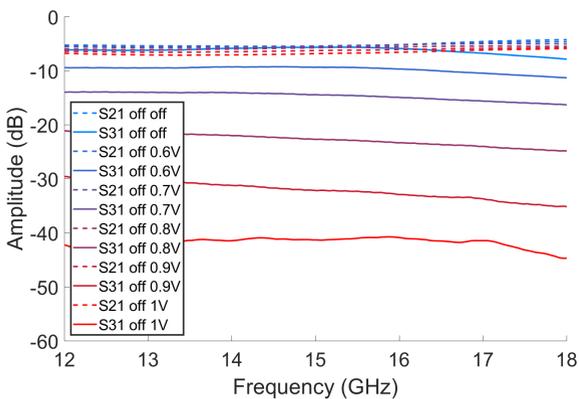


FIGURE 10. Transmission from port 1 to the ports 2 and 3 measured when the right attenuator is progressively biased.

port 3 when the attenuator of port 2 is biased. Some elements about explaining this phenomenon as well as the asymmetry between the attenuation of each port are suggested in the “Discussion” section.

The feeding network has also been tested in the linearity setup described in section II-C. The transmission is measured from port 1 to port 2, with port 3 being connected to a matched load. The measurements are presented in Fig. 11 (a) for compression and in Fig. 11 (b) for intermodulation. In accordance with the results of II.C, no non-linear behavior in compression nor intermodulation have been observed, and transmission levels are consistent with the low power measurements from Fig. 9 in all states.

E. ANTENNA

The antenna used is a dual-feed square patch, with each feed using quarter wavelength line matching as well as coupling matching. The geometry of the antenna and the matching elements are exposed in Fig. 12.

Circular and linear polarizations are obtained by changing the ports feed configuration. The simulated performance of the antenna shows a -10 -dB bandwidth of 400 MHz centered

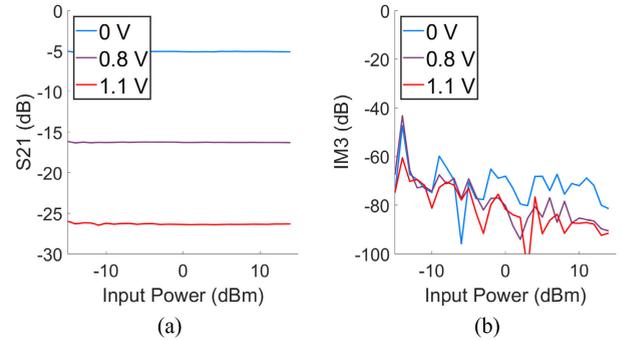


FIGURE 11. (a) Measured S_{21} through the feeding network under various bias conditions at 15 GHz with regards to input power. Port 3 is matched. (b) Measured third order intermodulation product relative power through the feeding network with regards to input power in 3 different states.

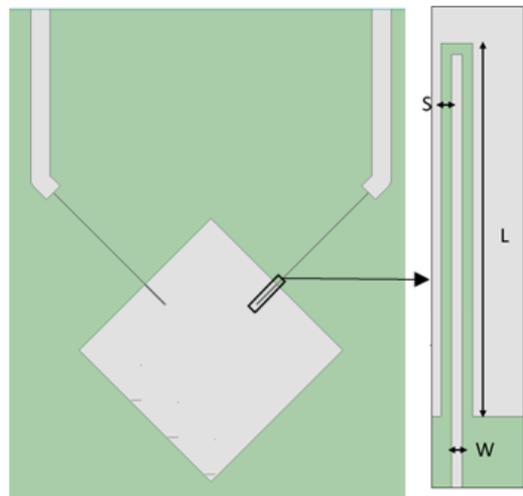


FIGURE 12. Antenna and coupled feed line dimensions. $S = 10 \mu\text{m}$, $L = 0.35 \text{ mm}$, $W = 10 \mu\text{m}$. The feed line is 1.777 mm long. Each side of the patch is 2.735 mm wide.

around 15 GHz (2.6 %), with a 2.8 dBi gain and a 6 dBi directivity.

F. POLARIZATION RECONFIGURABLE ANTENNA

A photograph of the manufactured device is shown in Fig. 13. The device fits in a $7 \times 7 \text{ mm}^2$ square, including the bias pads. The simulated and measured reflection parameter of the device is shown in different bias conditions in Fig. 14. In all states, a 2.6 % 10-dB bandwidth is measured. However, the resonant frequency of the H-LP state shifted to 15.3 GHz.

The simulated emission performance is shown in Fig. 15. The device allows for an axial ratio variation from 2.1 dB to more than 28 dB. The maximum gain is 2.5 dBi in the LHCP configuration. The gain in the H-LP and V-LP configurations are respectively 1.2 dBi and -0.1 dBi. A 3 dBi drop in gain is expected as only half of the power reaches the port for a given linear polarization.

A picture of the far field measurement setup is shown in Fig. 16. The antenna under test is connected to the VNA by

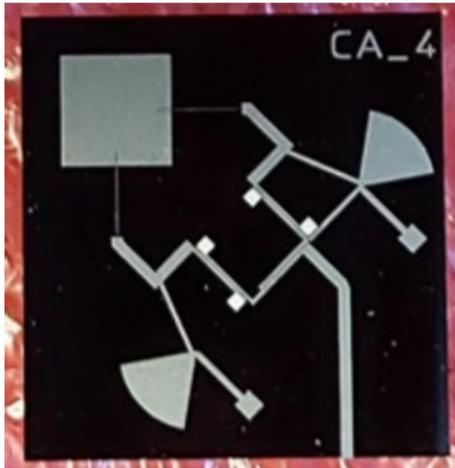


FIGURE 13. Photograph of the manufactured device.

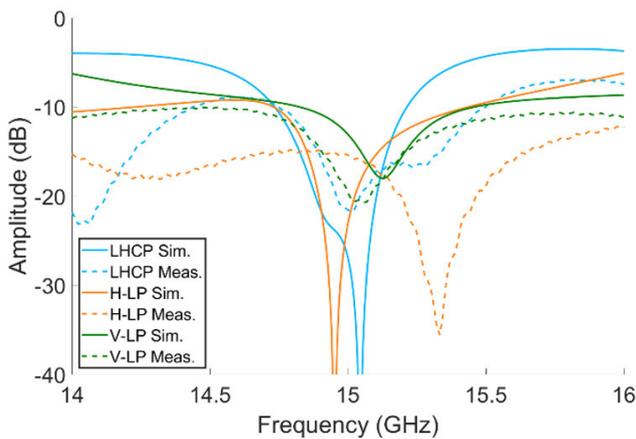


FIGURE 14. Simulated and measured S_{11} in the 3 extreme states.

a GSG probe. The reception horn antenna is fixed on a 6-axis robot arm. It allows for 360° rotation of the horn antenna pointing vertically in the direction of the antenna under test. The transmission parameter is then recorded on the VNA for each relative angle. Fig. 17 shows the normalized S_{21} transmission through a rotation of the horn antenna in the 3 states. The power reference is the maximum transmitted power measured during the reception antenna rotation. The axial ratio can then be extracted using the S_{21} fluctuation with regards to the angle between the antennas. The axial ratios measured in LHCP, H-LP and V-LP are respectively 3.8 dB, 16 dB and 20 dB.

III. DISCUSSION

The overall performance of the device is promising. The few discrepancies between simulations and measurements are explained as follows.

Firstly, a retro-simulation of the attenuator behaviour has been conducted using the COMSOL semiconductor and electromagnetism modules. The results in Fig. 18 (a) show that a significant reduction in resistivity occurs around each

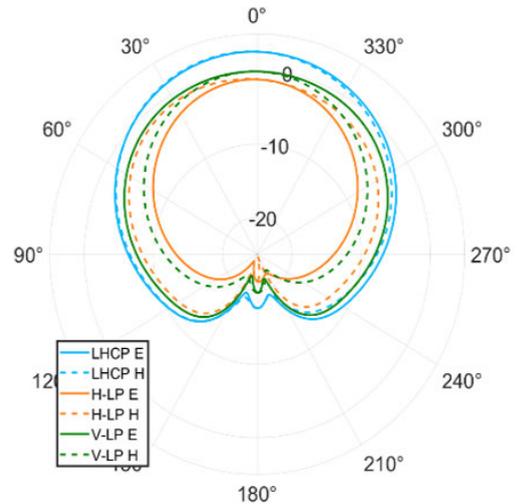


FIGURE 15. Simulated gain in the 3 extreme states in each plane.

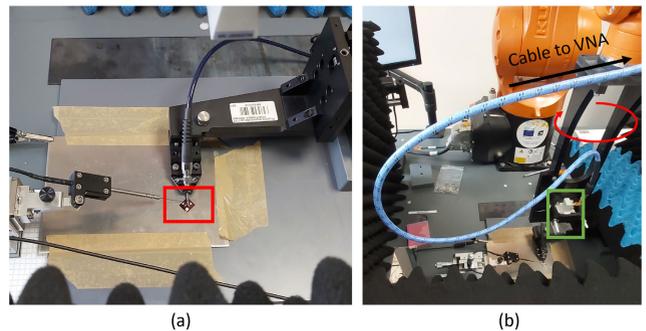


FIGURE 16. (a) Antenna (red box) on the measurement table connected to the RF probe on the coplanar port and the DC probe on the bias pad, (b) Overview of the measurement setup with the rotating robot arm holding the horn antenna (green box) pointing down 30 cm above the DUT.

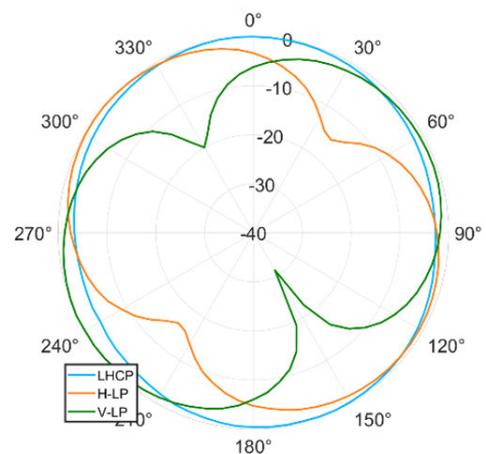


FIGURE 17. Measured normalized transmitted power fluctuations (dB) with regards to the angle between the antenna under test and the receiver horn antenna, for each bias configuration.

diode instead of being confined under the doped areas. The consequence of this phenomenon is the introduction

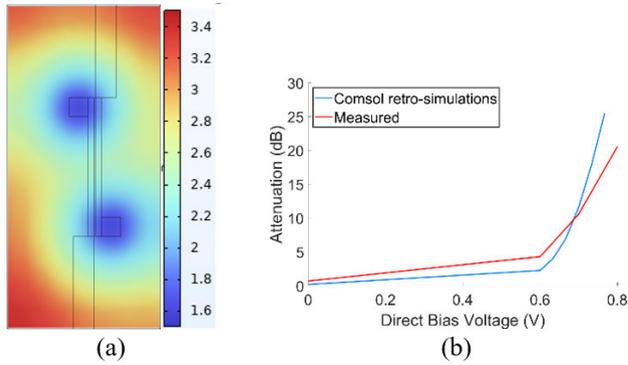


FIGURE 18. (a) Resistivity field (log ohm.cm) on a clip plane at half of the height of the substrate under 0.6 V direct bias, simulated on COMSOL semiconductor. (b) retro-simulated attenuation performance at 15 GHz compared to measured attenuation over a range of bias voltage.

TABLE 1. Comparison with similar devices.

Ref.	F ₀ (GHz)	Gain (dBi)	Polarized states	Normalized area (GHz ² .mm ²)
[3]	1.25		LHCP / RHCP	110x143
[4]	1.0/1.5		LHCP / RHCP	
[7]	2.1 / 3	2.8	LHCP / RHCP H-LP / V-LP	450x450
[10]	13.5 / 15	8 / 5 (2x2 array)	LHCP / RHCP H-LP / V-LP	615x390
[11]	5	6 (sim)	LHCP / RHCP	150x185
[12]	10.9 / 11.9	0.9 / 3.5 / 4.75	RHCP H-LP / V-LP	330x385
This work	15	2.5 / -1.2 (sim)	LHCP H-LP / V-LP	105x105

of additional losses to other components in proximity to the doped areas as seen on Fig. 8. Due to the location of the ScDDAs of the attenuator controlling the power to the port 3, the resistivity of the substrate under the input coupler is lowered when the attenuator is on high bias conditions, explaining the discrepancy.

Similarly, this layout disposition can explain the additional attenuation range towards port 3 as the input coupler introduces additional losses when the ScDDAs are on high bias conditions. This effect could be mitigated by adjusting the layout to spread the attenuators further away from the input coupler. The high matching between the measured and the retro-simulated attenuation curves in Fig. 18 (b) provide confidence in the retro-simulated model.

Lastly, the frequency shift between linear states and the increased axial ratio are due to a simulated phase accuracy issue, and retro-simulations showed consistent results after increasing convergence rules.

A further study evaluating the sensitivity of the ScDDAs with regards to temperature would be helpful to understand their behavior in various environments.

Overall, the device possesses competitive performance in frequency and integrability, fitting for use in all integrated high frequency agile antenna arrays as compared to previous works in Table 1, while also providing I/O active power level control functionality. The ScDDA approach allows for a high compactness, linearity, agility and high frequency while maintaining state-of-the-art emission performance and low manufacturing complexity compared to other integrated technologies.

IV. CONCLUSION

An all-integrated agile feeding network for a polarization-tunable antenna at 15 GHz on silicon is presented. Each part of the system has been simulated and measured for validation, as well as retro-simulations showing a deep understanding of the design and models. Power handling of ScDDAs have been investigated and show outstanding results in linearity. This work demonstrates the possibilities allowed by the all-integrated ScDDA design flow applied to tunable integrated devices beyond the traditional lumped component approach in modern front-end design.

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